ABSTRACT

COHERENCE CONTROLLER FOR A MULTIPROCESSOR SYSTEM,
5   **MODULE, AND MULTIPROCESSOR SYSTEM WITH A MULTIMODULE**
ARCHITECTURE INCORPORATING SUCH A CONTROLLER

The large-scale symmetric multiprocessor server with a multimodule architecture includes N identical multiprocessor modules 50, 51, 52, 53. The module 50 includes a
10   plurality of multiprocessors 60, 61, 62, 63 equipped with a cache memory and at least one main memory connected to a coherence controller 64 that includes an external port 99 connected to at least one of the multiprocessor modules 51, 52, 53 outside the module 50 and a cache filter directory 84 SF/ED designed to guarantee coherence between the mass memory and the cache memories of the modules, the cache filter directory 84 including a
15   local presence vector 86 that keeps track of the memory lines or blocks copied into the cache memories of the module 50 and an extension 88 that keeps track of the coordinates of the memory lines or blocks copied from the local module 50 to an external module 51, 52, 53.

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The Abstract relates to Fig. 2.